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Literature Review

Design and Synthesis of Windowed Watchdog Timer for High Speed Memory Applications

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Abstract

Because embedded systems are utilised in such a broad variety of security-related applications, it is imperative that they have an exceptionally high level of dependability in order for them to operate correctly. External watchdog timers are used in these systems so that time-related problems may be automatically handled and recovered from in the event that they arise. The bulk of the external watchdog clocks now available on the market have a limited number of activities that they can do since adjusting their timeout durations requires extra circuitry in most cases. A watchdog timer that has been developed and is suitable for use in memory-related applications such as data storage is discussed in this work. A Verilog HDL-based design was used to develop the system, and a Verilog-based simulation was used to create it using Xilinx ISE 14.7. Both of these were written in Verilog.

Keywords: Low Power VLSI; Windowed Watch Dog Timer; Memory

Introduction

Those individuals who are interested in learning how to design integrated circuits (ICs) should begin by gaining an understanding of integrated circuit design, which is a topic that falls under the umbrella of electronics engineering [1]. Integrated circuits (ICs) are created by using photolithography to arrange miniaturised electronic components on a monolithic semiconductor substrate into an electrical network [2]. This process results in the production of integrated circuits (ICs).

Integrated circuit design may be broken down into two basic categories: analogue integrated circuit design and digital integrated circuit design. Microprocessors, field-programmable gate arrays (FPGAs), memory (RAM, ROM, and flash), and digital application-specific integrated circuits (ASICs) are all examples of digital integrated circuits (ICs). When it comes to digital design, logical soundness, optimising circuit density, and designing circuits in such a manner that clock and timing signals are routed as effectively as possible are all very important considerations. In addition, analogue integrated circuit design places a significant emphasis not just on power IC design but also on radio frequency (RF) design [3,4]. Using analogue integrated circuit design, it is possible to build a wide variety of circuit components, including oscillators, active filters, linear regulators, phase-locked loops, and operational amplifiers, to name just a few. In the design of analogue circuits, elements like as gain, matching, power dissipation, and resistance are all properties of semiconductor devices that are becoming more important. Because analogue signal amplification and filtering must keep high levels of fidelity, analogue integrated circuits (ICs) typically use larger active components and less compact circuitry than digital integrated circuits [5]. This is because analogue signal amplification and filtering must maintain high levels of fidelity.

Literature Review

Title of the paper	Author's name	Publisher	Contribution
FPGA Implementation of an improved watchdog timer for safety and critical applications	R. Unni,, P. Vijayanand, Y. Dilip	Jan 2018 IEEE	This paper describes the architecture and design of an improved configurable watchdog timer that can be employed in safety-critical applications. fault detection mechanisms are built into the watchdog, which adds to its robustness
Fault detection mechanism using improved watchdog timer for safety and critical applications	K. V. Krishna, H. V. Sahana	July 2021 IJRESM	The effective of the proposed watchdog timer to detect and respond to faults. The fault detection mechanisms built in to the watchdog, the implementation of the watchdog timer in FPGA.
An improved watchdog timer to enhance imaging system reliability in the presence of soft errors	Ashraf M. El- Attar, Gamal Fahmy	January 2008 IEEE	The problem of standard and windowed watchdog timers is also solved with a new watchdog timer system. A single counter is all that is needed to improve watchdog timer fault coverage with the new architecture.

Table 1

Basic of watchdog timer

There are a variety of timeout lengths available for standalone timer microchips that are less generic in nature. The addition of additional circuitry to other devices can be used to change the timeout periods of the devices in question [6,7]. While this strategy is effective, it increases the complexity of the hardware and the overall cost ofthe system, despite its effectiveness. The use of a Field Programmable Gate Array (FPGA) to build external watchdogs can reduce both the cost and the complexity associated with their implementation (FPGA). Today's embedded systems rely on FPGA chips to perform critical functions, which are found in a wide range of applications [8]. With the help of an FPGA, it is possible to design a watchdog timer that is both efficient and reliable. The watchdog processor for real-time control systems on FPGAs such as Giaconia, etc., was investigatedin this paper. As an alternative to providing the CPU with a timer, a reasonableness check on selected variables was carried out, as well as a simple programme flow inspection. El-Attar and colleagues pushed for the use of time register-based sequenced watchdog clocks to identify when a malfunction has occurred in a computer system.The software's defect-detection abilities are very limited, making it impossible to customise the software's features. To keep things as simple as possible, the authors concentrated on the fundamentals of an FPGA watchdogtimer system that makes use of a large number of hardware timers [8].

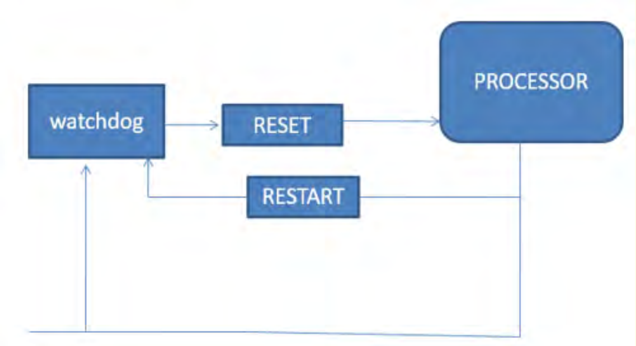

Figure 1: Watchdog timer.

Watchdog timer input–output interface and configuration Register

Admittedly, this article works deal with covers the fundamental and scope of the watchdog timer. The block diagram of the watchdog timer is presented in figure 2.

Watchdog timer architecture

When a problem arises, the WDT immediately steps in to monitor and troubleshoot the situation. The timer circuit,which is generally composed of a processor, needs to be reset periodically by the

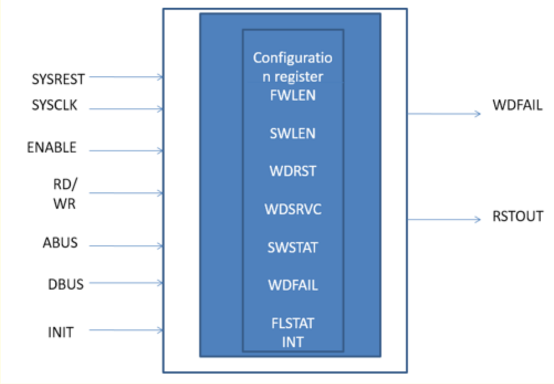

Figure 2: Block diagram of the Watchdog timer.

processor. The WDT expires asa secondary indicator of a problem with the system being investigated. When the watchdog fails to reset, the CPUis restarted or put into a known condition from which it can recover. It's possible to have a processor's watchdog built in (on-chip) or external. However, the use of internal watchdogs is not a guaranteed method of simplifying and saving money on hardware. The watchdog timer can be disabled by a runaway code since it is controlled by the software while it is running. When a crystal fails, the watchdog will be unable to perform its primary duty ofchecking for hardware malfunctions. When the reliability of an embedded system is at stake, external watchdogsare necessary. Existing system block diagram is presented in figure 3.

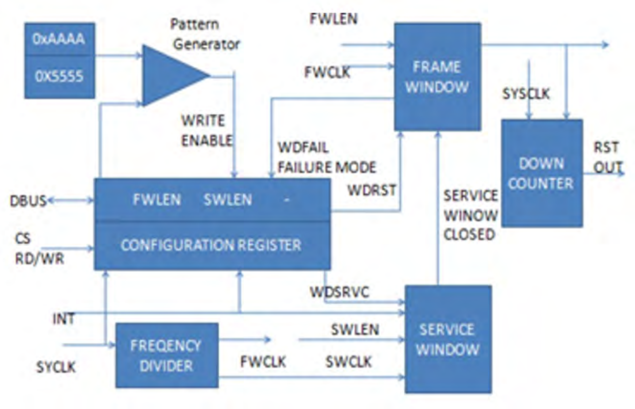

Figure 3: Existing system architecture of watchdog timer.

Monitoring software that does its job well should be able to detect and restore the system's normal operating modes. Is it possible to reset all peripherals on timeout? The suggested watchdog timer relies on a separate clockto perform its functions. To start up, the design uses a windowed watchdog implementation in which the windowdurations can be set. Whenever a watchdog timer expires, a fail flag is raised, and the timer is reset after a predetermined amount of time. During this time, a non-volatile storage medium can be used to store useful debugging information. The proposed system watchdog timer is presented in figure 4. In figure 5 presented the memory application block diagram.

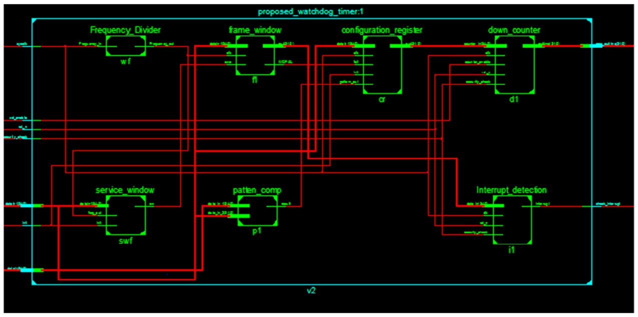

Figure 4: Proposed watchdog timer for memory applications.

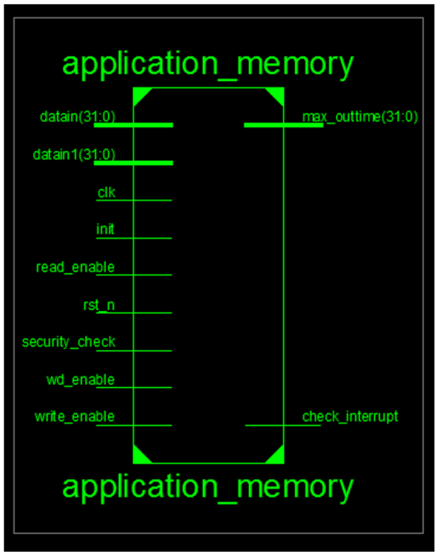

Figure 5: Application memory.

Simulation Results

When the watchdog is powered on or reset, the WDFAIL output is set to a high voltage. The watchdog must be started and maintained by the software itself. How the watchdog reset is set up, as well as how it functions in general, may be seen in the waveform shown in figure 6. In figure 7 depict the RTL diagram of watchdog timer. The configuration register WDRST must be changed from low to high in order for the watchdog to function properly. When this is completed and the watchdog's service window has expired, the WDFAIL flag will be de-asserted and the watchdog will resume its normal operation. As long as the frame window is kept open for a longer period of time than the system frame duration, a new service window will be initiated before the current frame window expires, and so on. After the watchdog has been properly serviced once more, the frame window will be re-initialized to its original state. For as long as the counters on the frame window frames are operational, the watchdog will not report any malfunctions. Technology schematic diagram is presented in figure 8.

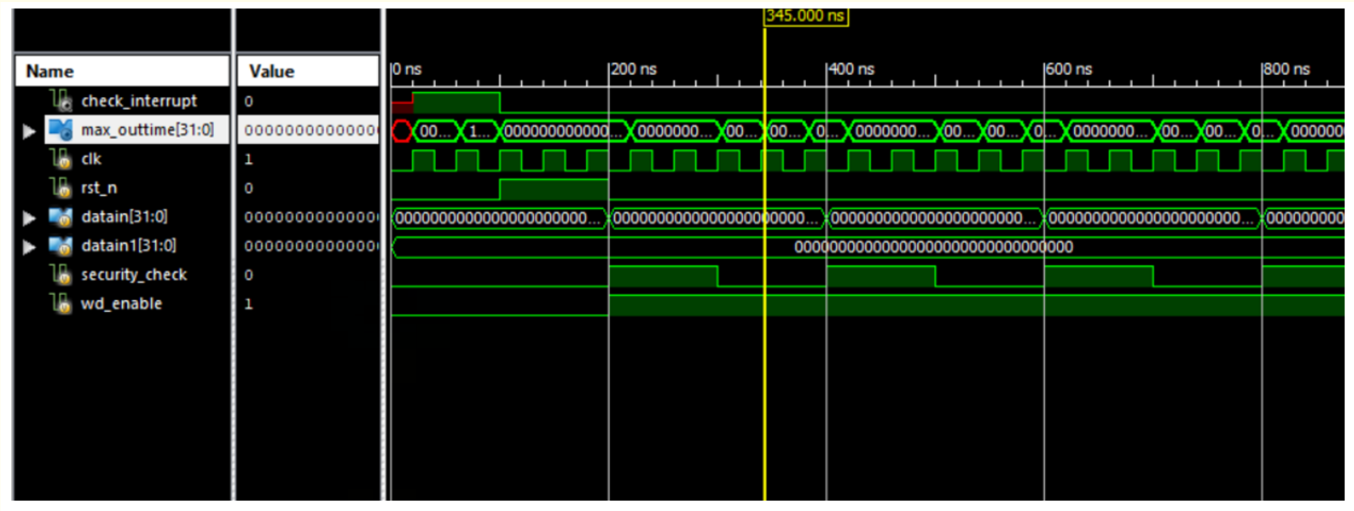

Figure 6: Simulation waveforms.

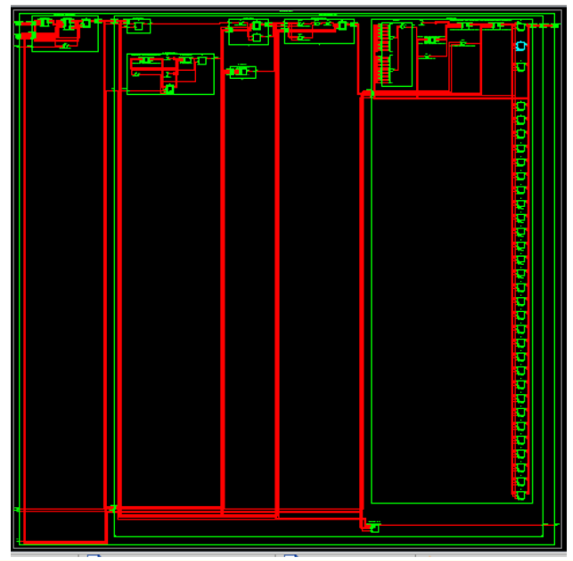

Figure 7: RTL SCHEMATIC.

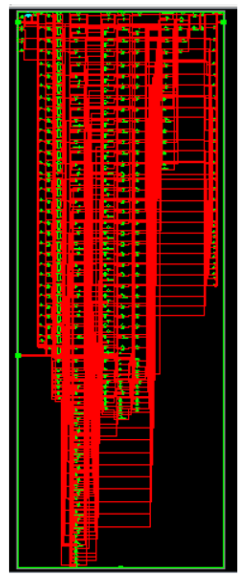

Figure 8: Technology Schematic.

Conclusion and Future Scope

We have developed a Watch Dog timer that uses the user's previous experiences as its primary data source. In order to ensure the integrity of the memory, the parameters of the watch dog's specs were analysed and integrated into various applications. The Verilog HDL was used in order to develop this architecture, and the Xilinx ISE14.7 was utilised in order to synthesise it. Both of these programmes may be found on the Xilinx website. When developing an efficient watchdog system, it is very necessary to give careful consideration to both the software and the hardware. As was just said, it is essential to give considerable thought, in advance, to what would be the most effective response to take in the event of a crisis. We have identified the source of the problem. A watchdog might be of assistance to you in enhancing the design of your product. When it comes to the hardware, you need to come to a conclusion as quickly as possible after buying it. You will be rewarded for your forward thinking and ability to plan. Having a system that is more robust comes with a number of benefits.

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