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Editorial

Low Cycle Fatigue in Solder Joint Interconnections of IC Devices: Could it be Avoided?

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"Do not go where the path may lead, go instead where there is no path and leave a trail".

Ralph Waldo Emerson (1803-1882)

Reliability physics undertakings are usually based on establishing the weakest link in the designs and technologies of importance and to make sure that this "link" is sufficiently reliable for the given device and application. Solder joint interconnections (SJIs) is the most vulnerable structural element in the IC products. It is usually perceived, that, because of the inevitable thermal contraction mismatch of the dissimilar materials in the design, it is impossible to avoid inelastic strains in it, and, because of that, also the highly damaging low cycle fatigue conditions in the solder material. Various modifications of Coffin-Manson empirical relationships are widely employed today to evaluate its useful lifetime. It has been recently shown, however [1], that an attempt to avoid inelastic strains in the SJIs of IC devices and packages and, hence, - low cycle fatigue conditions in this material is not at all hopeless. This could be done by combining one or more of the following design means: using low soldering temperatures; and/or high yield stress solder; and/or by selecting low CTE substrates, for better CTE match with Si; and/or by using SJIs with elevated stand-off heights (such as, e.g., column grid array (CGA) designs, instead of ball-grid-array (BGA) designs); and/or employing inhomogeneous solder systems, in which relatively stiff joints are used in the major mid-portion of the assembly, where good heat transfer performance is critical, and compliant joints or even epoxy adhesives - at the assembly's peripheral portions, where strength considerations are of the paramount importance. The inhomogeneous design could be optimized, by selecting, for the given materials, the lengths of the peripheral zones, in such a way that the maximum interfacial shearing stresses at the assembly ends become equal to the stresses at the boundaries between the mid-portion of the assembly and its peripheral portions. Calculations indicate that the stresses in such an optimized assembly are considerably lower than the stresses in an assembly with an homogeneous attachment, even if a compliant BGA is employed. One could use the following simple formula to tentatively check, if an attempt to avoid inelastic strains at the ends of the design might be successful: $l_Y = \frac{1}{k}\left(\frac{\tau_e^{\infty}}{\tau_Y} - 1\right)$. Here τ_e^{∞} is the maximum interfacial shearing stress, assuming that the solder material is ideally elastic, τ_Y is the yield stress (in shear) for the given solder material, $k = \sqrt{\frac{\lambda}{\kappa}}$ is the easily calculated parameter of the interfacial shearing stress. It depends on the axial, λ and the interfacial, k compliances of the assembly. If the calculated l_Y values are negative, this means that no inelastic strains are likely to occur.